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THE DIRECT TELEMETRY ENCODER:

A DETAILED DESCRIPTION

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Fernando Antonio Pessotta

Responsible author

14. Abstract/Notes

This document presents a detailed description of the Direct Telemetry Encoder for the data collection satellite. The Encoder acquires 72 digital and 96 analog telemetry signals from the satellite subsystems.

The acquired data is formated in a 128 octet frames.

The telemetry frames are continuosly generated producing a bit stream of 2048 bps. The bit string is biphase encoded and modulates a 65.536 kHz square wave subcarrier in PSK, producing the telemetry video that is sent to S-band transponder.

15. Remarks

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MDB/SS	PÁGINA: i
	VERSÃO: 01

TÍTULO

A DETAILED DESCRIPTION

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ASS.	NOME	/ / DATA

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DIRECT TELEMETRY ENCODER

1 - INTRODUCTION

Basically the Direct Telemetry Encoder (CODIR) is a unit that acquires telemetry signal, formats the acquired telemetry in frames and sends them to the S-Band transponder and the umbilical connector.

The data from the subsystems is sent to two sets of multiplexers both inside the CODIR. The first set is controlled by the CODIR and the second one is controlled by the UAC of the UPD/C which receives the corresponding multiplexed output.

The telemetry data acquired from the subsystems by the multiplexer under CODIR control is formatted in a 128 octet frame as depicted in Figure 1.

0	1	2	3			126	127
SYNC	SYNC	MODE AND FRAME #	FORMAT #	TELEMETRY DATA (108 OCTETS)	SPARE (14 OCTETS)	CRC	CRC

Fig. 1 - CODIR Telemtry Frame

The telemetry frames are continuously generated at a rate of two frames per second producing a bit stream of 2048 bps. The bit string is biphase encoded and modulates a 65.536 kHz square wave subcarrier in PSK, producing the telemetry video that is sent to the S-Band transponder and to the umbilical connector.

The CODIR consists of a controller, three Analog Interfaces and two Digital Interfaces. The block diagram of the CODIR is presented in Figure 2.

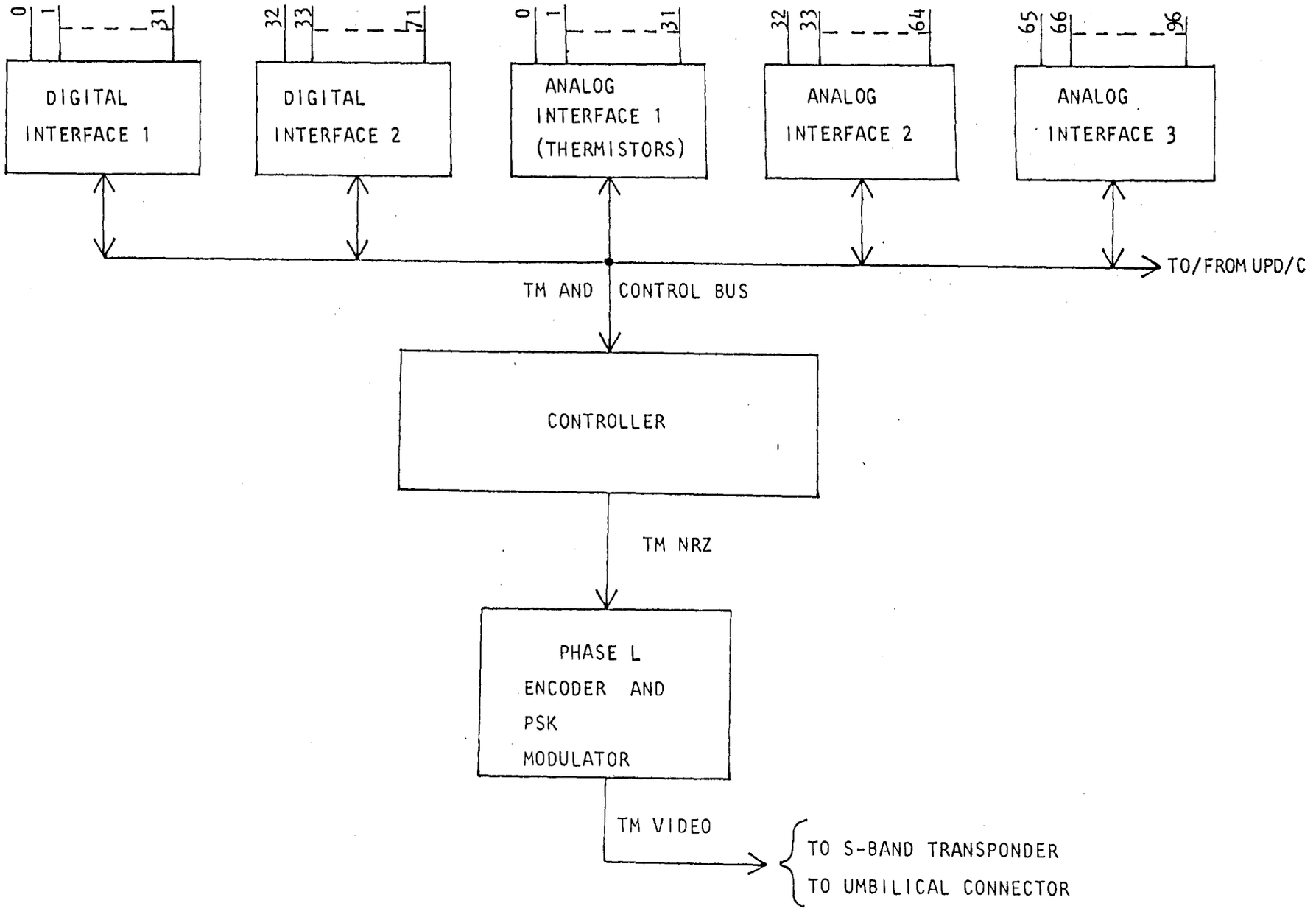


Fig. 2 - Direct Telemetry Encoder Block Diagram.

2 - CONTROLLER

The controller provides the address for externa multiplexers, converts the analog telemetry signals in to digital ones and formats the acquired telemetry in frames, adding a header and CRC to the beginning and end of frame, respectively.

The block diagram of the controller is presented in Figure 3.

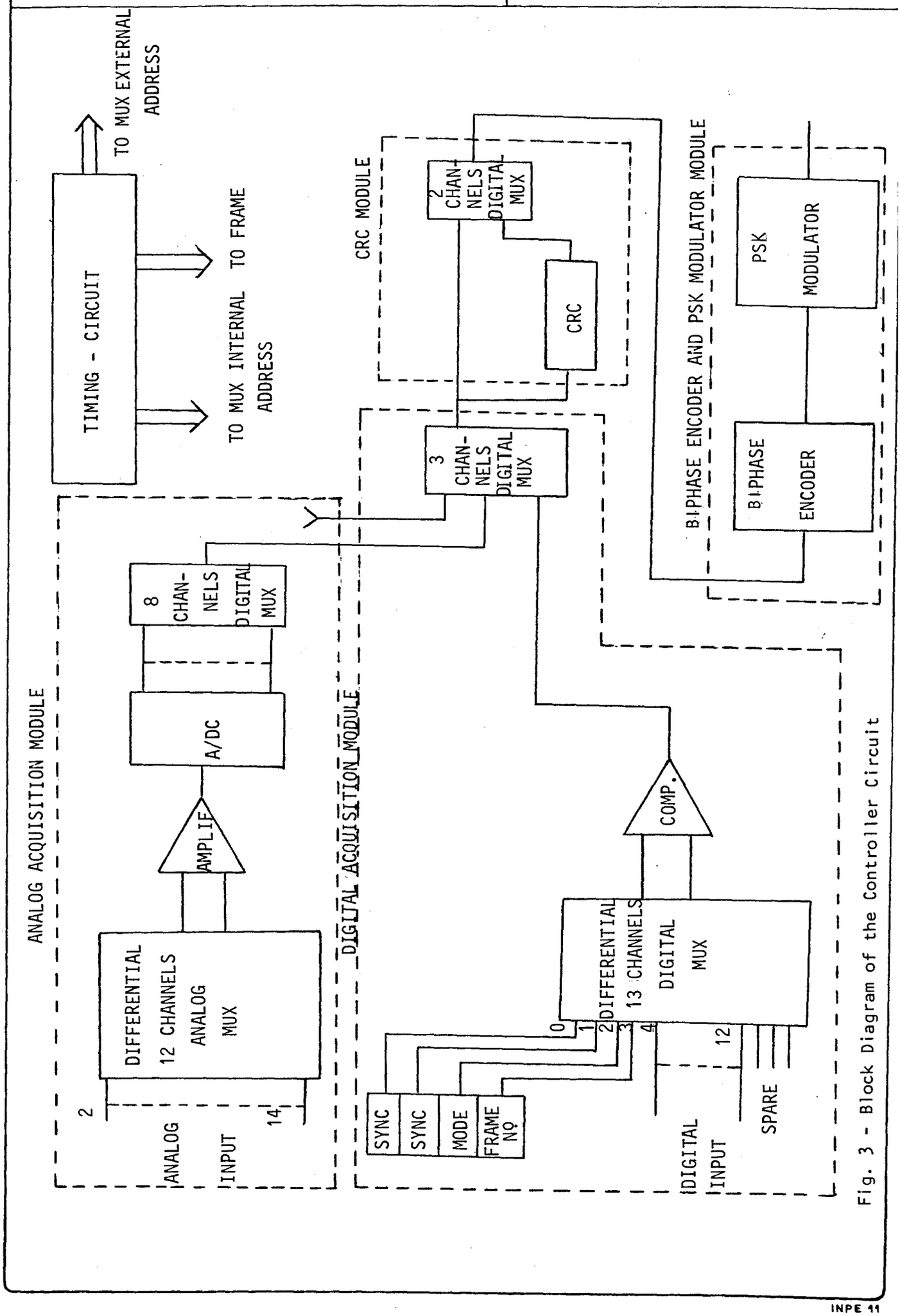


Fig. 3 - Block Diagram of the Controller Circuit

2.1 - TIMING CIRCUIT

This circuit is composed of a 131.072 kHz oscillator and a set of counters that supply the internal and external multiplexer address and the 8 - bit frame number.

2.2 - ANALOG ACQUISITION MODULE

This module consists of 12 - channels differential analog multiplexers, an amplifier, an A/D converter and an 8 - bits digital multiplexer. Each analog input receives eight analog signals multiplexed in the analog interface. The differential multiplexer output is amplified to adapt the input signal level to the A/D converter.

The amplifier circuit is presented in Figure 4.

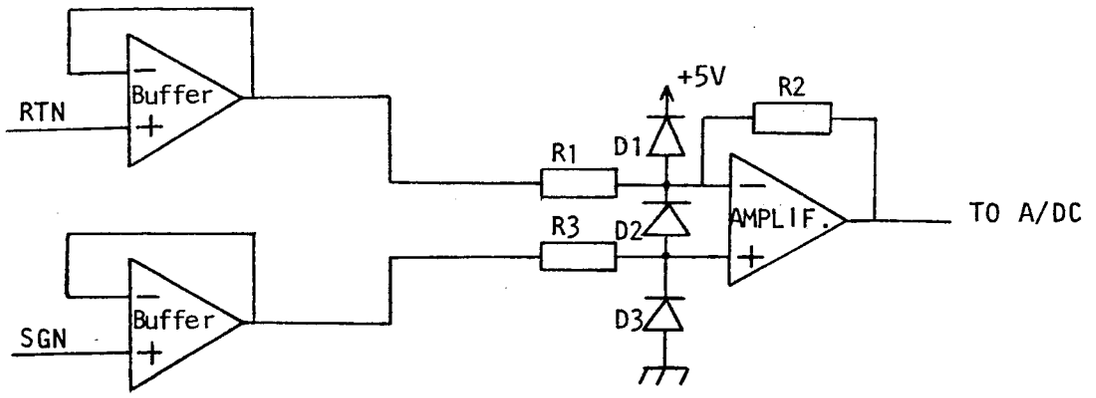


Fig. 4 - Diagram of Amplifier

The two voltage followers are utilized to provide a high input impedance. The input voltage is limited by the diodes and the gain of the differential amplifier is two.

The A/D converter is based on AD 571 manufactured by Analog Devices. This A/D is a 10 bits converter, but only the 8 most significative bits are used. The A/D input range is programed to 0v to 10v and the conversion time is 25 μseg.

The A/D output is serialized by 8 channel digital multiplexers.

2.3 - DIGITAL ACQUISITION MODULE

This module consists of a 9-channel differential analog multiplexer, a comparator circuit, four 8-channel digital multiplexers and a 3-channel digital multiplexer.

The four 8-channel multiplexers provide the syncronism word (16 bits), the mode (8 bits) and the frame number generated by the timing circuit.

Each input channel of the differential digital multiplexer receives 8 digital signals multiplexed in the digital interfaces.

The differential multiplexer outputs are applied to a comparator circuit, described in Figure 5.

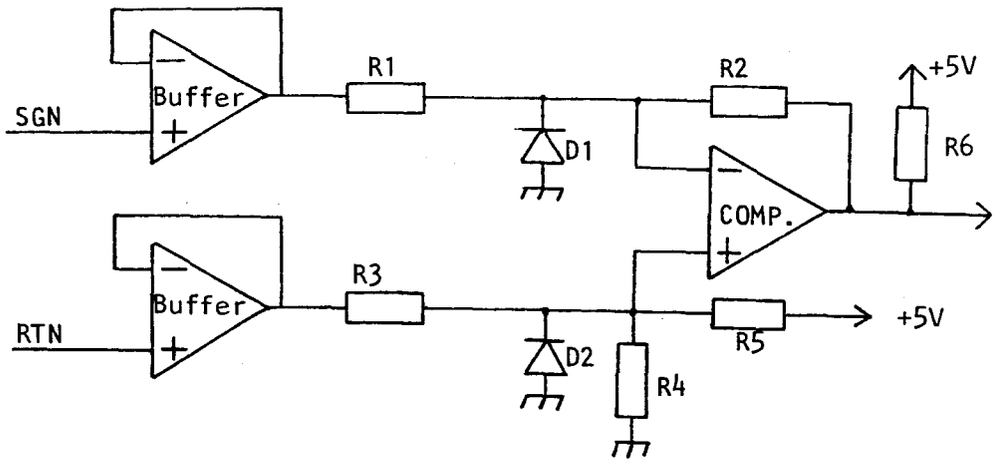


Fig. 5 - Diagram of Comparator Circuit.

The voltage followers are utilized to provide a high input impedance. The comparator is utilized to provide 2v of threshold to discriminate the digital levels.

The diodes protect the comparator against negative voltage.

The 3 channel digital multiplexers sequence the signal from digital and analog acquisition modules and spare signals (a 112 bits sequence of zeros and ones).

2.4 - CRC MODULE

that is trasm. This circuit generates a 16-bits, cyclic redundant code word during the trasmission of the telemetry frame to ground. The generation of the CRC begin as soon as the synchronism word is transmitted. The polynomial selected for the CRC is $G(x)= x^{16}+ x^{12}+ x^{5}+ 1$.

2.5 - BIPHASE ENCODER AND PSK MODULATOR MODULE

This circuit encodes the telemetry bit stream in a biphase L using a clock of 2048 HZ (see Figure 6).

The glitches generated in this circuit are eliminated by flip-flop of the PSK modulator circuit.

The stream bit from biphase encoder modulates a subcarrier of 65,536 KHz in PSK as presented in Figure 6.

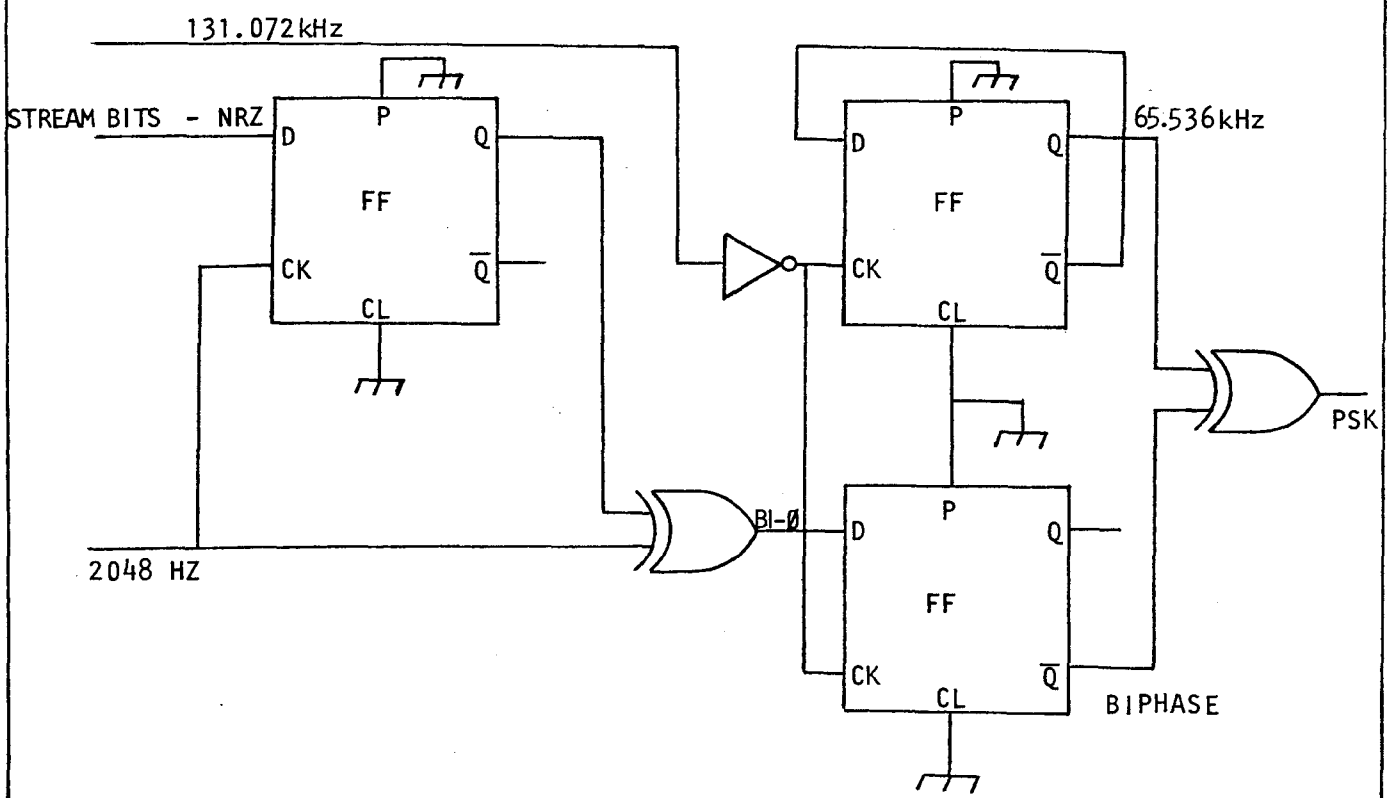


Fig. 6 - Diagram of BiPhase Encoder and PSK Modulator Circuits.

The circuit and timing diagram of controller are presented in Appendix A.

3 - DIGITAL INTERFACE I

The Digital Interface I consists of two sets of 32-channels differential multiplexers. The first set is addressed by the CODIR controller, while the second set is addressed by UAC of the UPC. Each digital telemetry input is sent to the two set of multiplexers that can be energized and operated independently.

The 1 MΩ resistor in the input of the multiplexers are utilized to protect the input against over voltage and to isolate the multiplexers controlled by the CODIR from the multiplexers controlled by the UAC of the UPD/C.

The differential multiplexers are used in order to isolate the ground among the subsystems and to reject the common mode noise.

The Digital Interface I circuit is presented in Appendix A.

4 - DIGITAL INTERFACE II

The Digital Interface II is similar to Digital Interface I. The only difference is the number of input channels, that is 40.

This interface also contains the comparator circuits to receive the multiplex address from the UAC of the UPD.

The digital interface II circuit is presented in Appendix A.

5 - ANALOG INTERFACE I

This interface is utilized to multiplex the 32 signals from the thermistors. In this interface, it is not necessary to multiplex the return of the thermistor because they have the same reference point. The thermistor circuits (Figure 7) are energized independently of the CODIR.

The Analog Interface I circuit is presented in Appendix A.

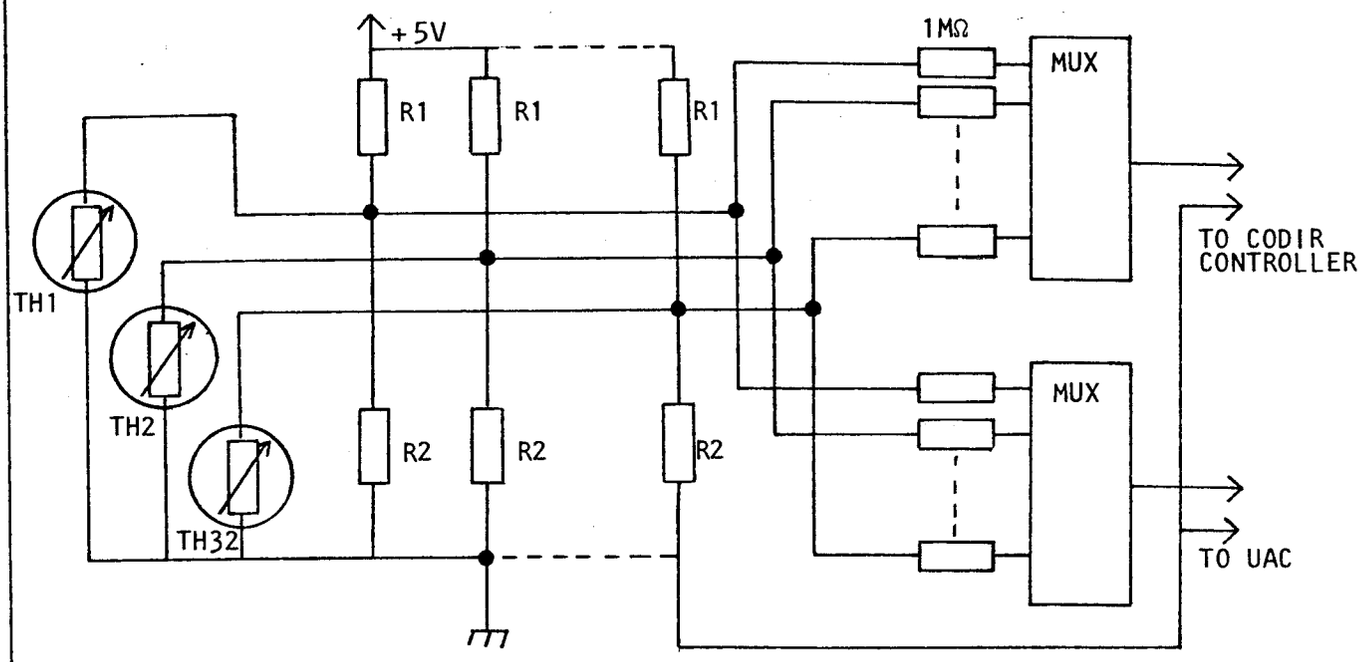


Fig. 7 - Temperature Acquisition Circuit.

6 - ANALOG INTERFACE II AND III

These interfaces are utilized to acquire the analog telemetry from subsystems. Each interface has the capability to acquire up to 32 channels.

In a similar way to the digital interface, the differential multiplexers are utilized to isolate the ground among the subsystems and to reject the common mode voice.

The Analog Interface II and III circuits are presented in Appendix A.

COMPONENTS LIST OF CONTROLLER

QTY	DISCRIPTION OF COMPONENT	PART NUMBER
	Analog Digital Converter	AD571SD-883
	Cristal Oscillator CMOS Frequence 131.072 kHz	CO.422D-2B
	3 Terminal Negative Regulators	LM79M05H03A
5	Diode High - Speed Switching	1N4148
	Resistor 5K1Ω; 1/8 W, 5%	
20	Resistor 10KΩ, 1/8 W, 5%	
5	Resistor 6K2, 1/8 W, 5%	
	Resistor 510KΩ, 1/8 W, 5%	
2	Resistor 2,5MΩ, 1/8 W, 5%	
	Resistor 5,1 MΩ, 1/8, 5%	
	Disc Ceramic Capacitor 33PF	
10	Disc Ceramic Capacitor 100 KPF	
3	D- Type Flip-Flop	4013B
6	Binary with asynchronous clear	40161B
5	8 Channel Data Selector	4512B
8	Analog Multiplexer/Demultiplexer	4051B
2	Quad Exclusive - or Gate	4070B
3	Nand Gates Quad 2 - INPUT	4011B
	And Gate Triple 3-input and Gate	4073B
2	Dual 4 - Stage Static Shift Register	4015B
	8 - Input nor/or Gate	4078B
	8 - Input Nand/and Gate	4068B
	Hex High-to-Low voltage (inverter)	4049VB
	Low Power Low off set voltage Quad Comparator	LM139AJ14A
4	Voltage Follower CER. Dip	LM110J14A
	Operational Amplifier	LM101AJ14A

COMPONENTS LIST OF DIGITAL I INTERFACE

QTY	DESCRIPTION OF COMPONENT	NUMBER PART
18	Analog Multiplexer/Demultiplexer	4051B
	3 - Terminal Negative Regulators	LM79M05H03A
128	Resistor 1MΩ , 1/8W, 5%	
	FC Printed Circuit Board Connectors	FC0801-120-00
6	Resistor 2KΩ , 1/8W, 5%	
6	Resistor 3KΩ , 1/8W, 5%	
6	Disc Ceramic Capacitor 220 PF	
6	Disc Ceramic Capacitor .33MF	
6	Disc Ceramic Capacitor .1MF	

COMPONENTS LIST OF DIGITAL II INTERFACE

QTY	DESCRIPTION OF COMPONENT	NUMBER PART
22	Analog Multiplexer/Demultiplexer	4051B
2	Low Power Low off set voltage Quad Comparators	LM139AJ14A
	Nand Gates Quad 2 Inputs	4011B
14	Resistor 5K1Ω, 1/8W, 5%	
21	Resistor 10KΩ , 1/8W, 5%	
160	Resistor 1MΩ , 1/8W, 5%	
	Disc Ceramic capacitor .33MF	
	Disc Ceramic capacitor .1MF	
	FC Printed Circuit Board Connectors	FC0801-120-00

COMPONENTS LIST OF ANALOG I INTERFACE

QTY	DESCRIPTION OF COMPENENT	NUMBER PART
10	Analog Multiplexer/Demultiplexer	4051B
32	Thermistor	
66	Resistor 1MΩ, 1/8 W, 5%	
32	Resistor , 1/8 W, 5%	
32	Resistor , 1/8 W, 5%	
	F.C. Printed Circ. Board Connectors	FC0801-120.00

COMPONENTS LIST OF ANALOG II INTERFACE

QTY	DESCRIPTION OF COMPONENT	NUMBER PART
18	Analog Multiplexer/Demultiplexer Single 8 - Channel	4051B
128	Resistor 1MΩ, 1/8 W, 5%	

COMPONENTS LIST OF ANALOG III INTERFACE

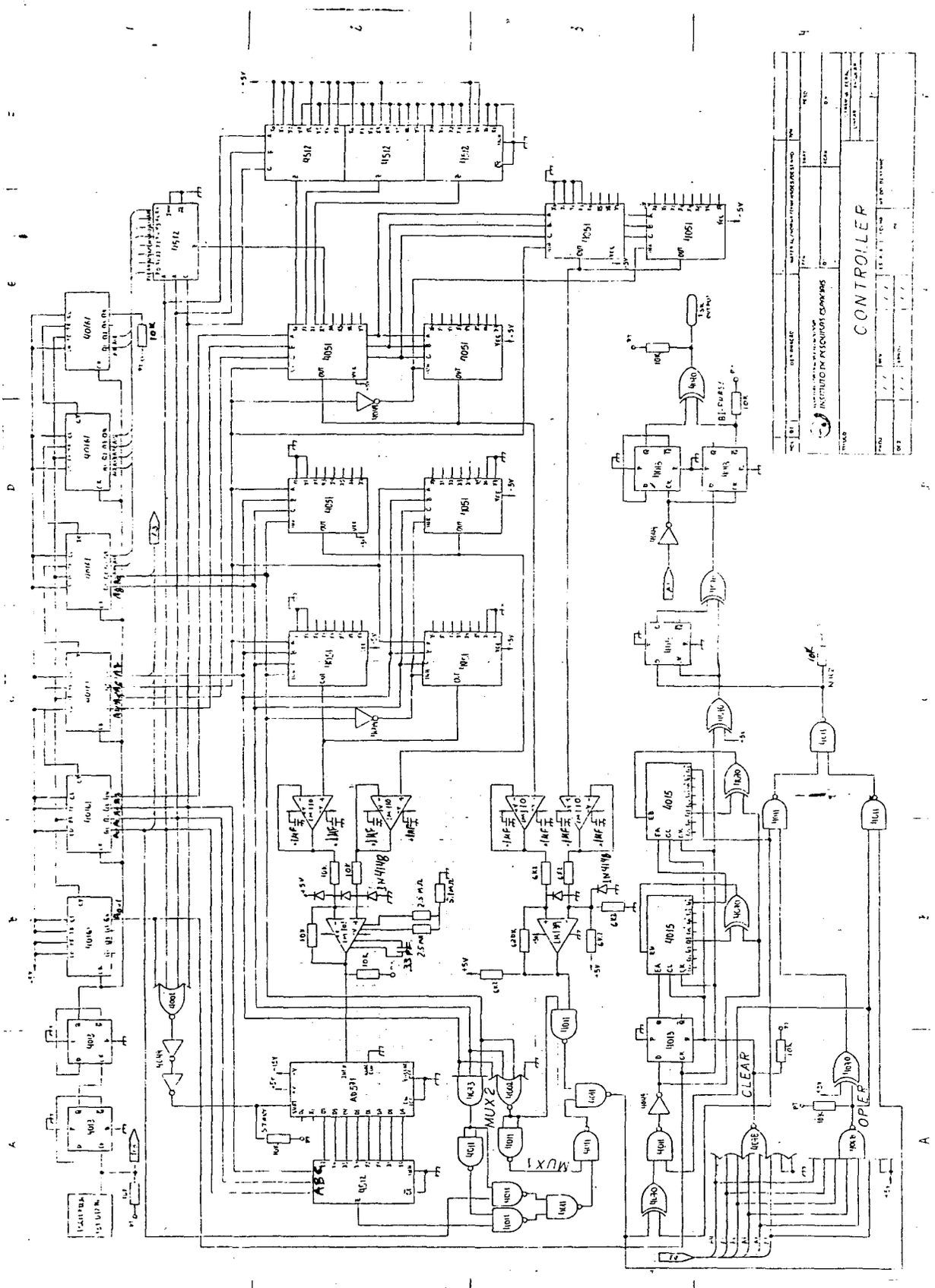
QTY	DESCRIPTION OF COMPONENT	PART NUMBER
18	Analog Multiplexer/Demultiplexer Single - 8 channel	
128	Resistor 1MΩ, 1/8W, 5%	
	FC Printed Circ. Board Connectors	FL0801-120-00

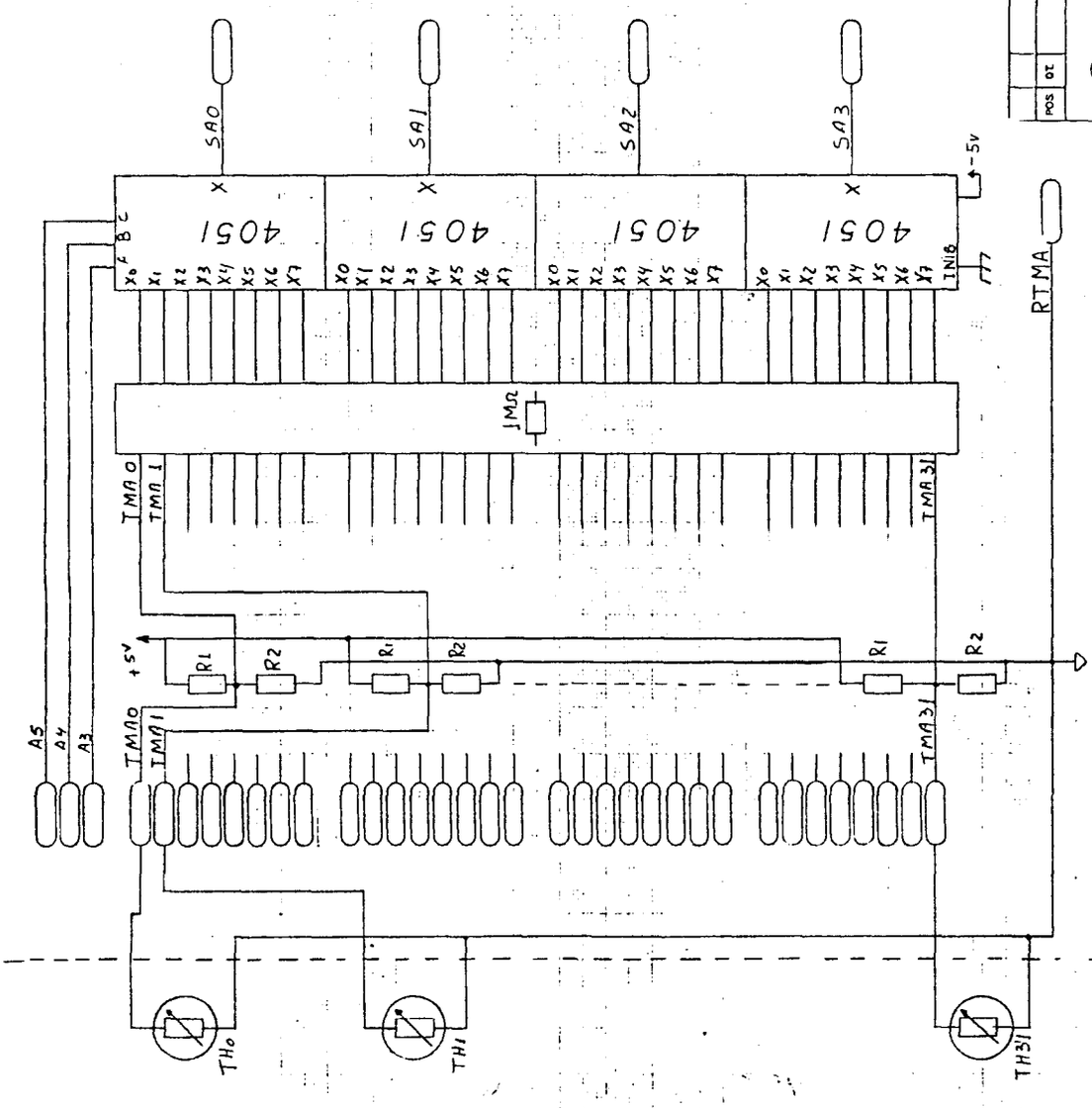
WIRING, CABLING SUBSYSTEM AND CONNECTORS AND ACCESSORIES

QTY	DESCRIPTION OF COMPONENT	PART NUMBER
	Stranded Hook-up wires 26 AWG	
	For Signal Lines	
	Stranded Hook-up wires 22 AWG	
	For Power Lines	
6	Rectangular D Subminiature	MD308N50P1
	Rectangular D Subminiature	MD308N37P1
6	Nylon Potting Shells	DD50908-1
	Nylon Potting Shells	DC50907-1
6	Switching Shells	DD19678-9
	Switching Shells	DC19678-8
	Screw Lock assembly	
6	FD Printed Circuit Board Connector (Receptor)	FD0301-120.00

APPENDIX A

ELECTRIC DIAGRAMS

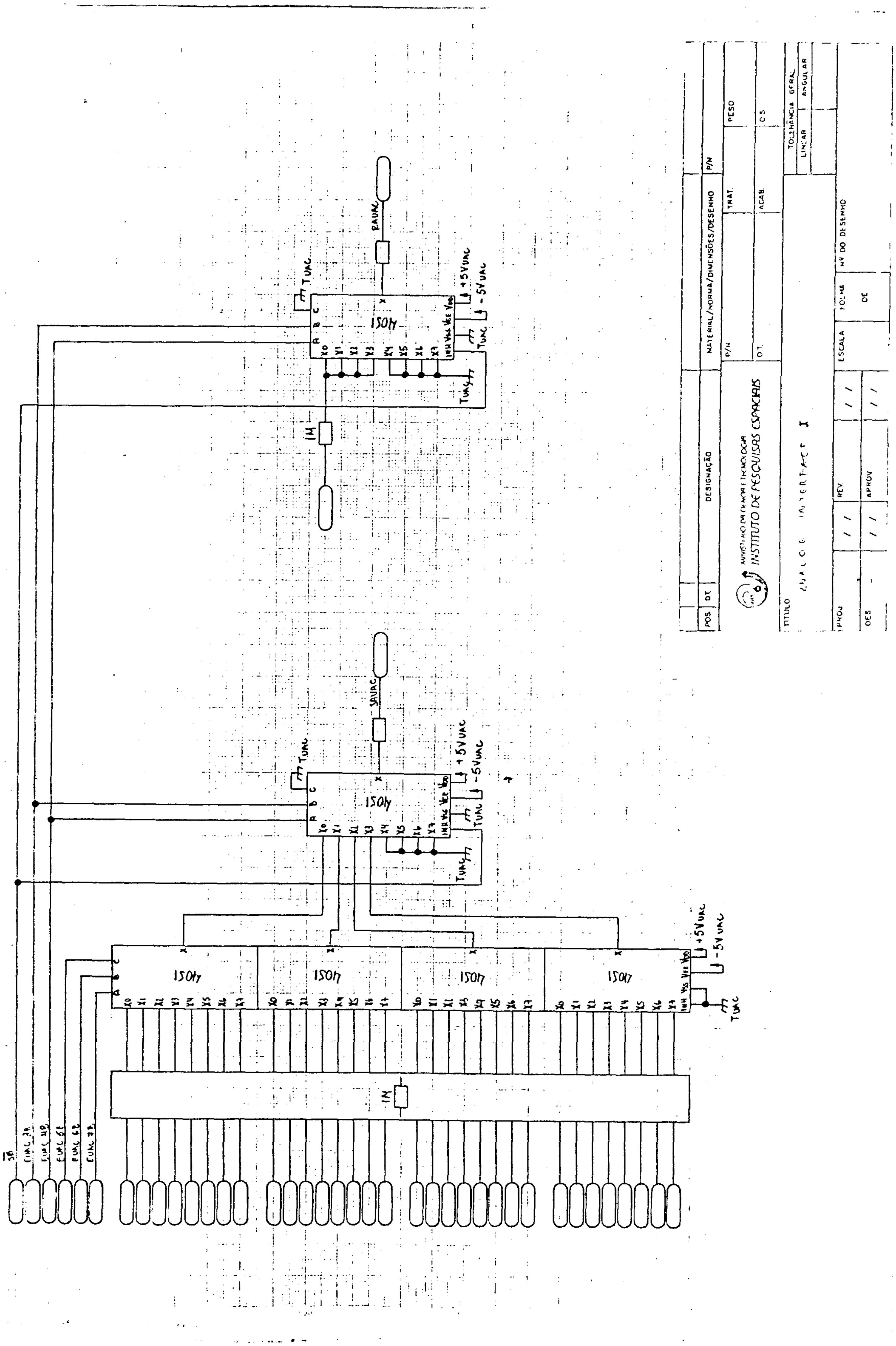

CONTROLEP
MUX2
MUX1
CLEAR
OPLEP

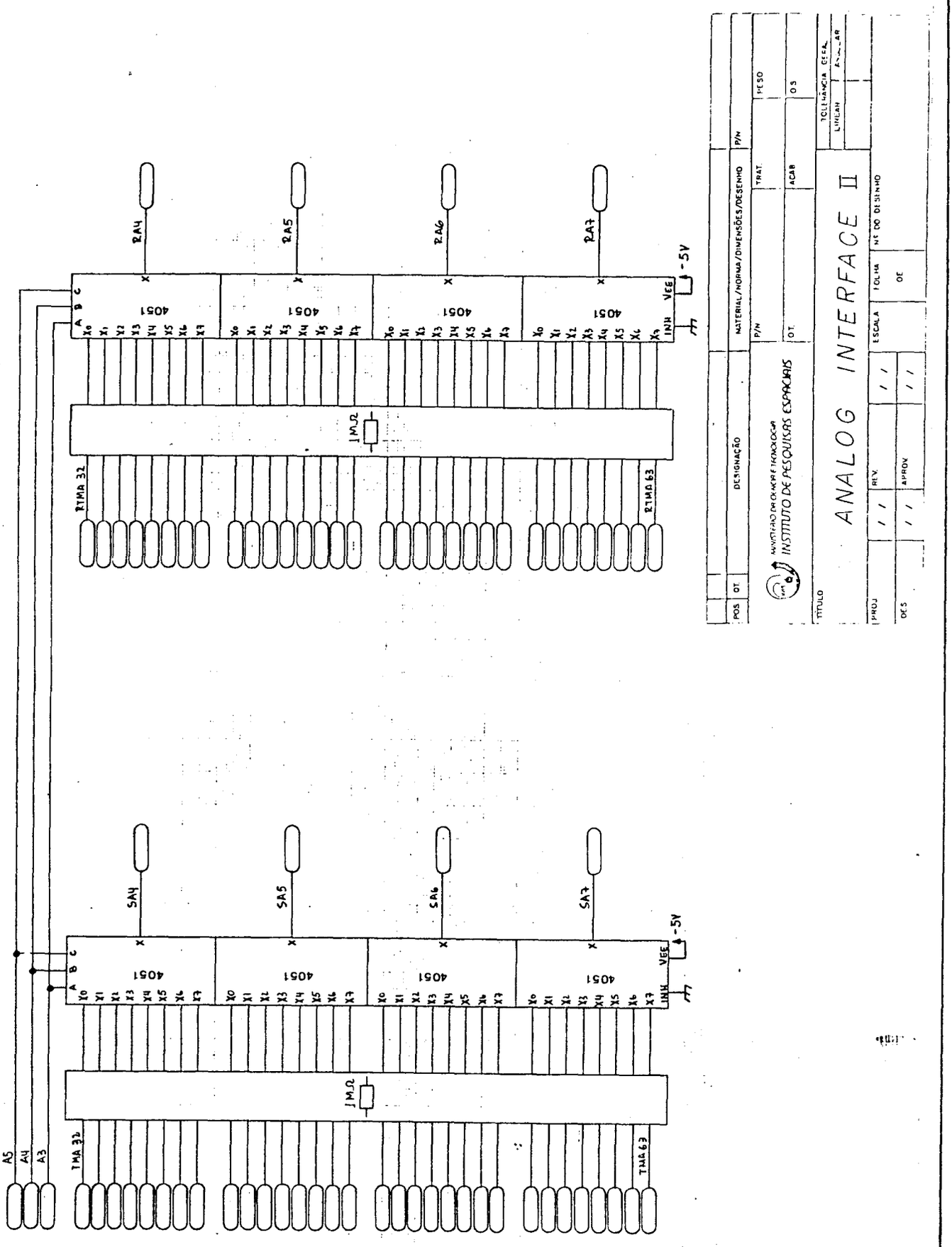

SA0
SA1
SA2
SA3
4051
+5V
RTMA
TMA0
TMA1
TMA31
R1
R2
A5
A4
A3
TH0
TH1
TH31

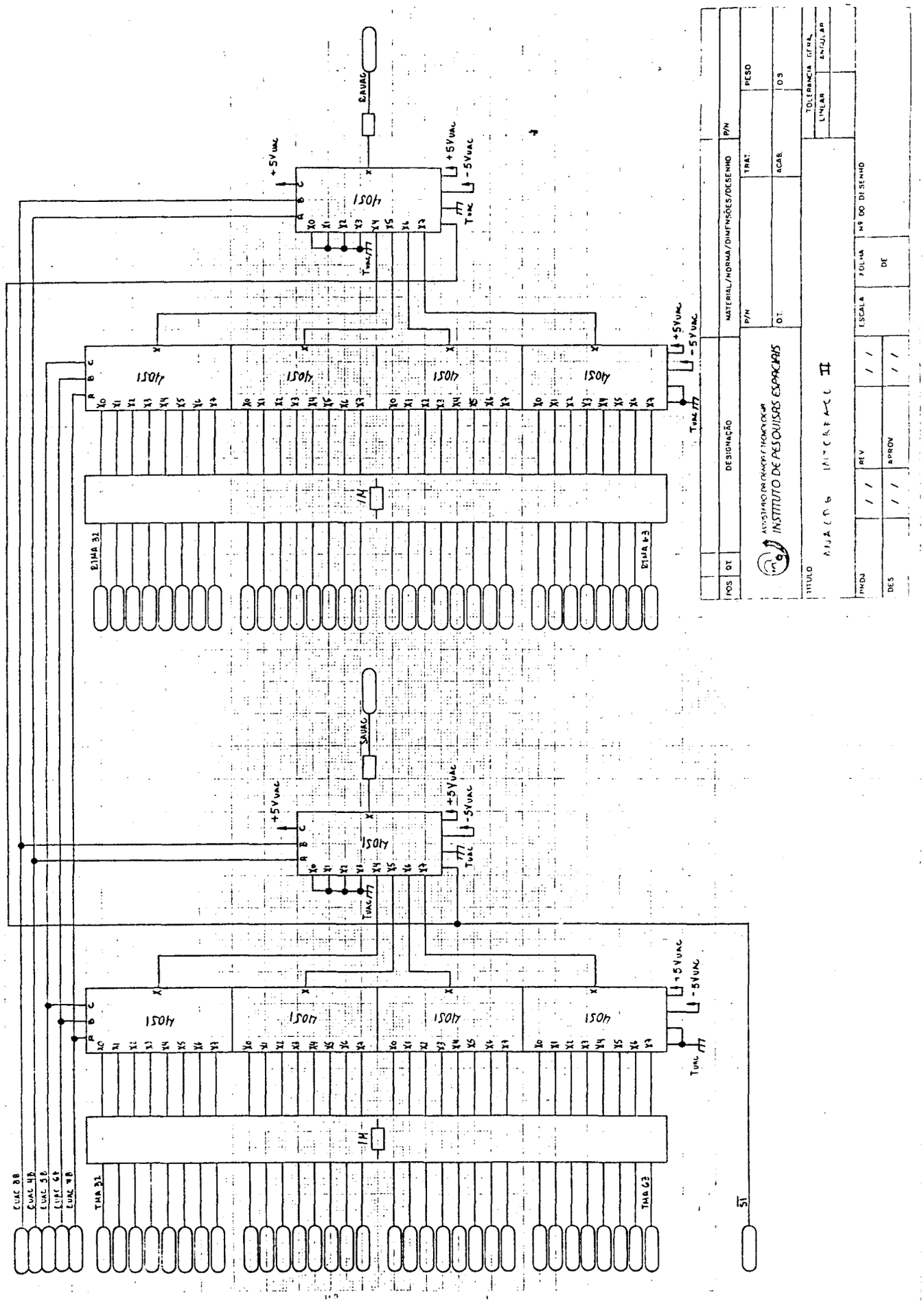
MINISTÉRIO DA CIÊNCIA E TECNOLOGIA
INSTITUTO DE PESQUISAS ESPACIAIS

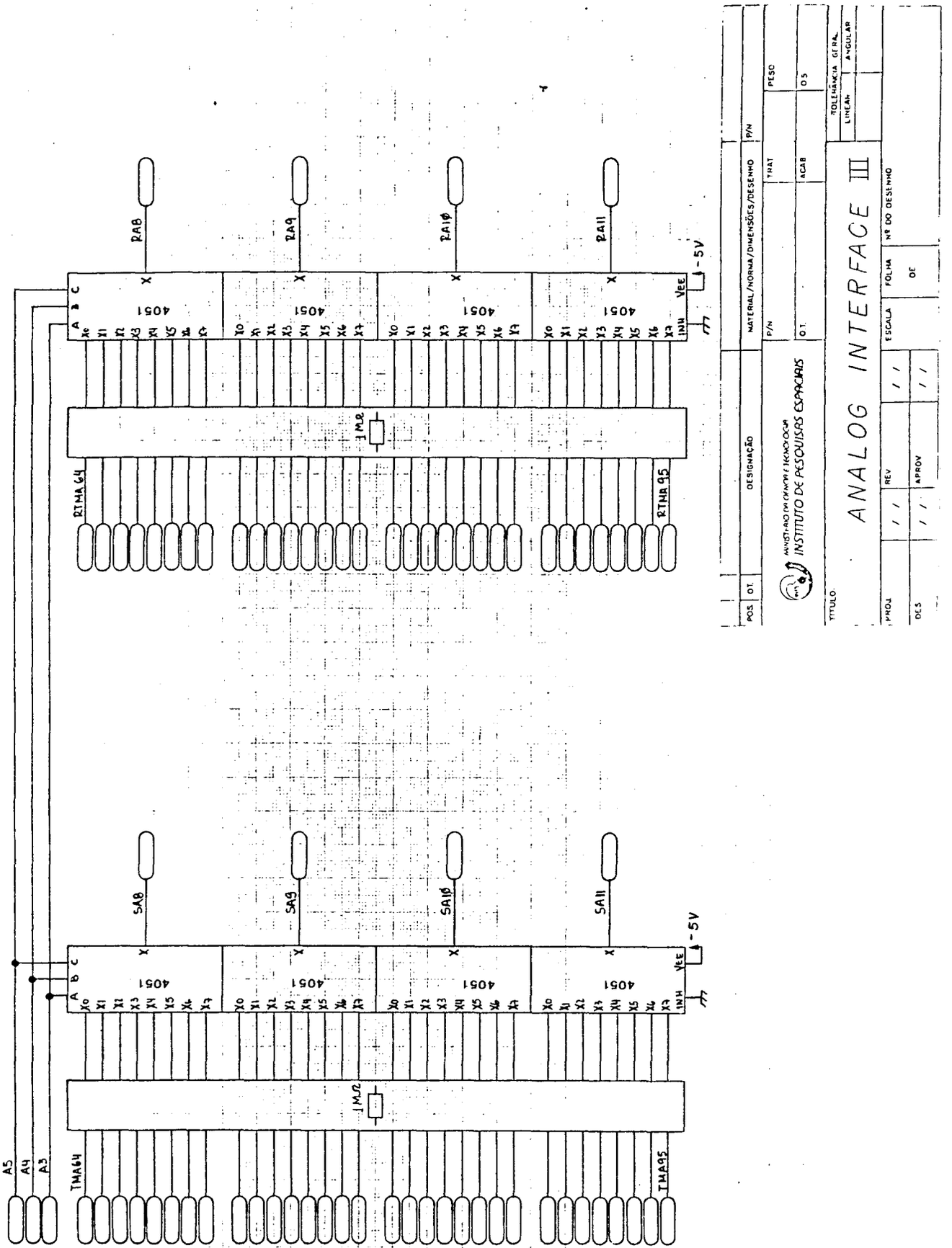
MECB/SS

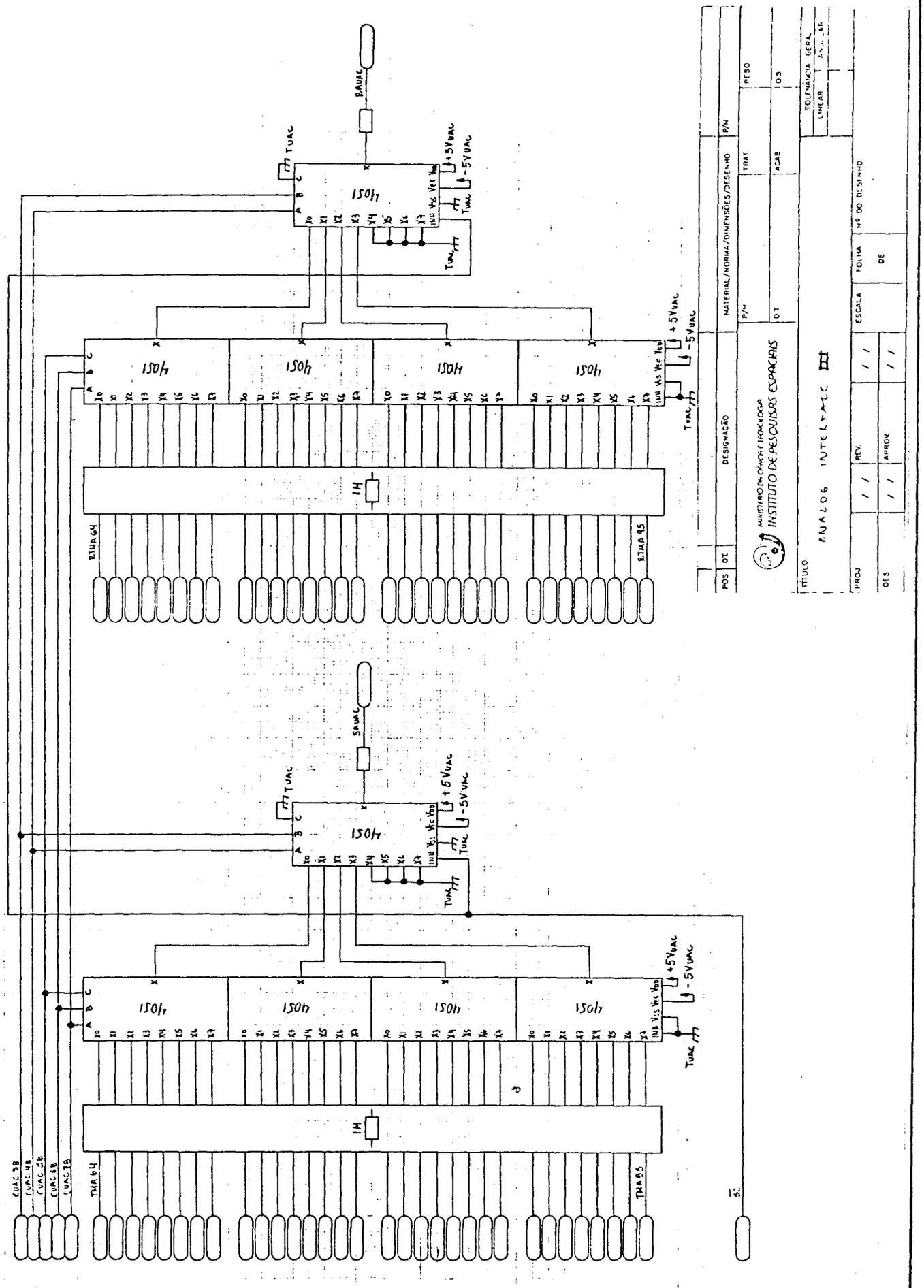
DOCUMENTO Nº: A-REV-0011
PÁGINA: A.4
VERSÃO: 01

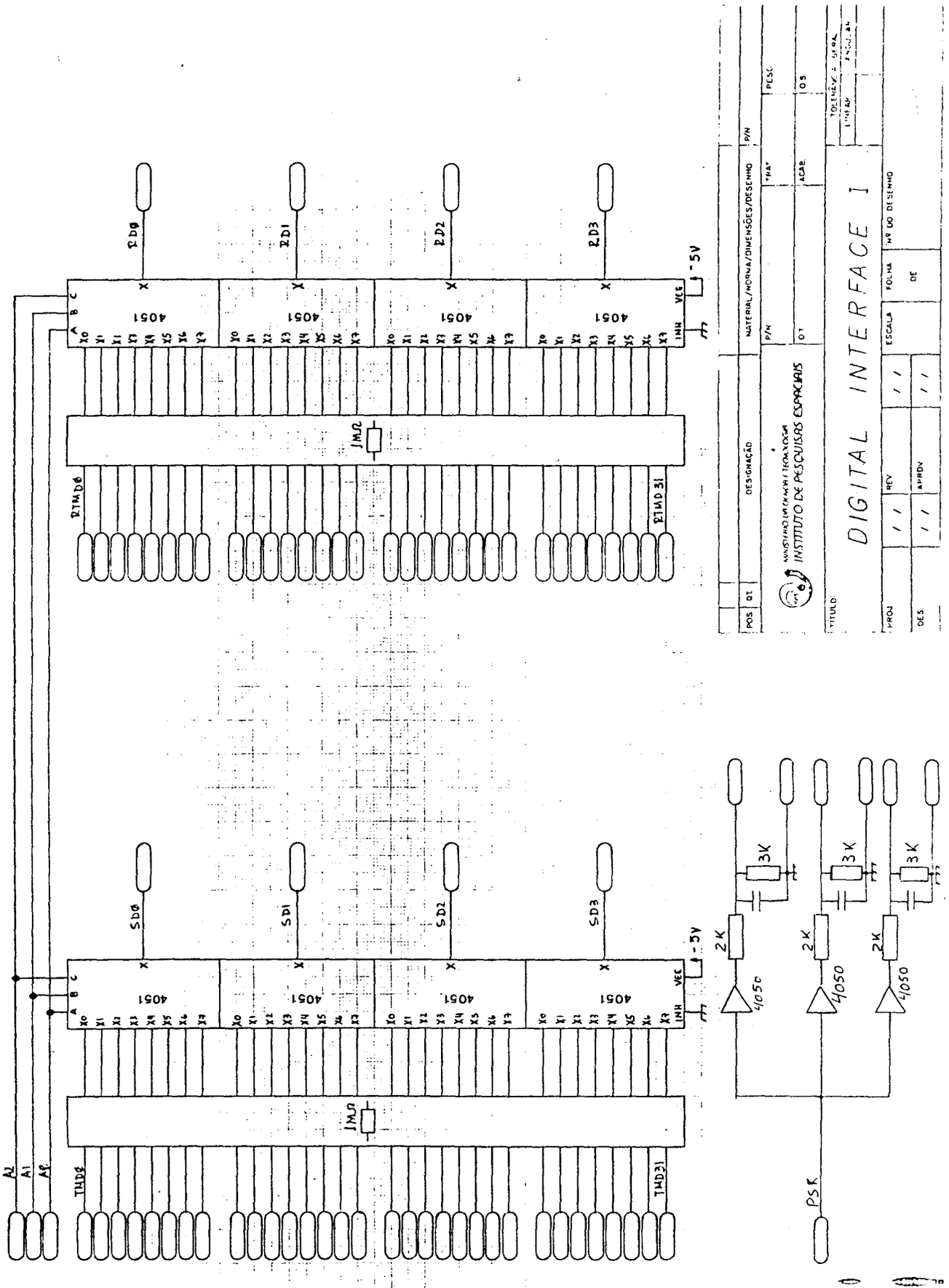


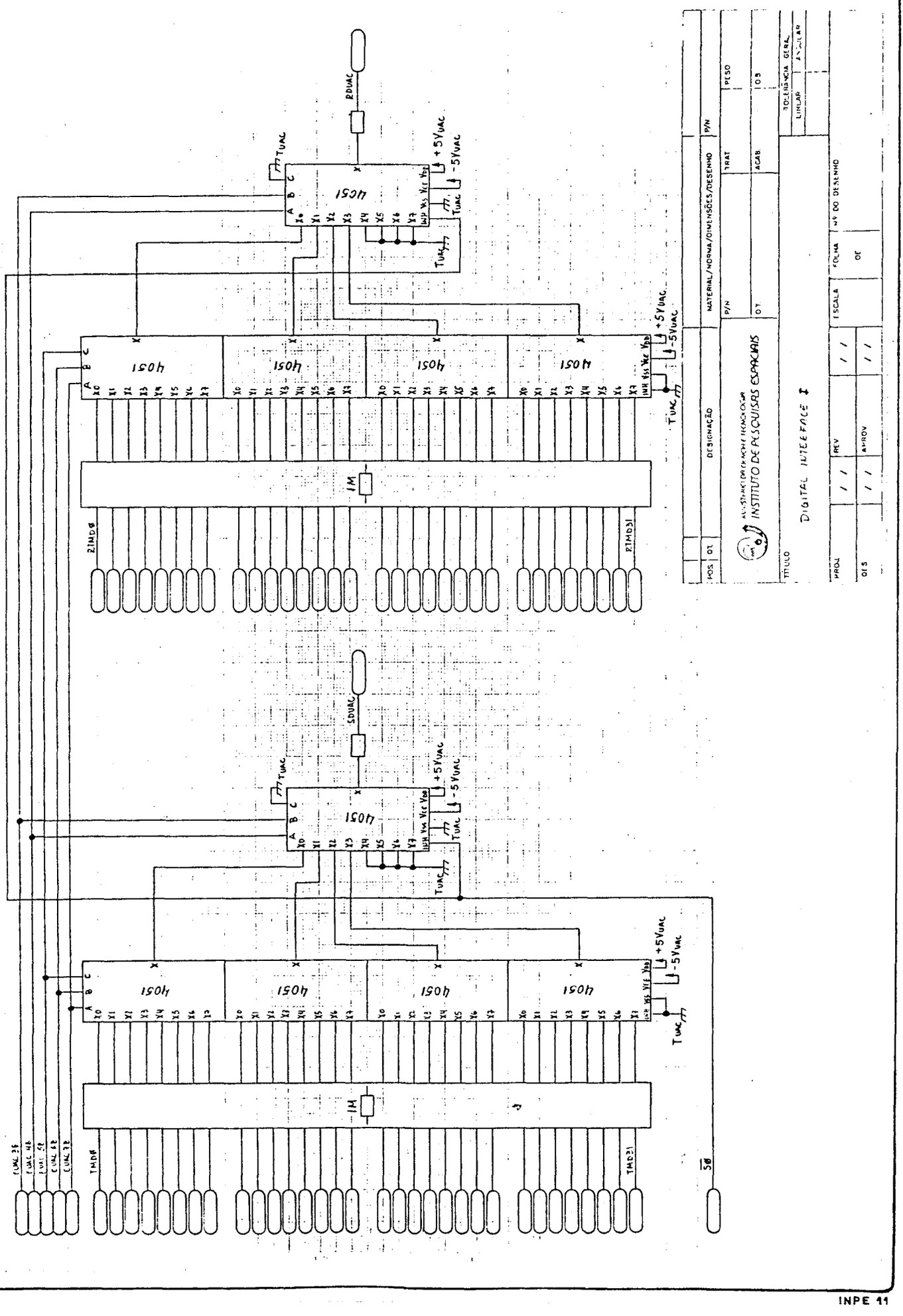

RA4
RA5
RA6
RA7
4051
A B C
X0 X1 X2 X3 X4 X5 X6 X7
INH
VEE
-5V
JMJ2
RMA 32
RMA 63
SA4
SA5
SA6
SA7
TMA 32
TMA 63
A5
A4
A3
POS
OT
DESIGNAÇÃO
MATERIAL/NORMA/DIMENSÕES/DESENHO
P/N
TRAT
ACAB
PESO
OS
TOLERÂNCIA GERAL
LINEAR
ANGULAR
INSTITUTO DE PESQUISAS ESPACIAIS
TÍTULO
ANALOG INTERFACE II
PROJ
DES
REV
APROV
ESCALA
FOLHA
OF
Nº DO DESENHO

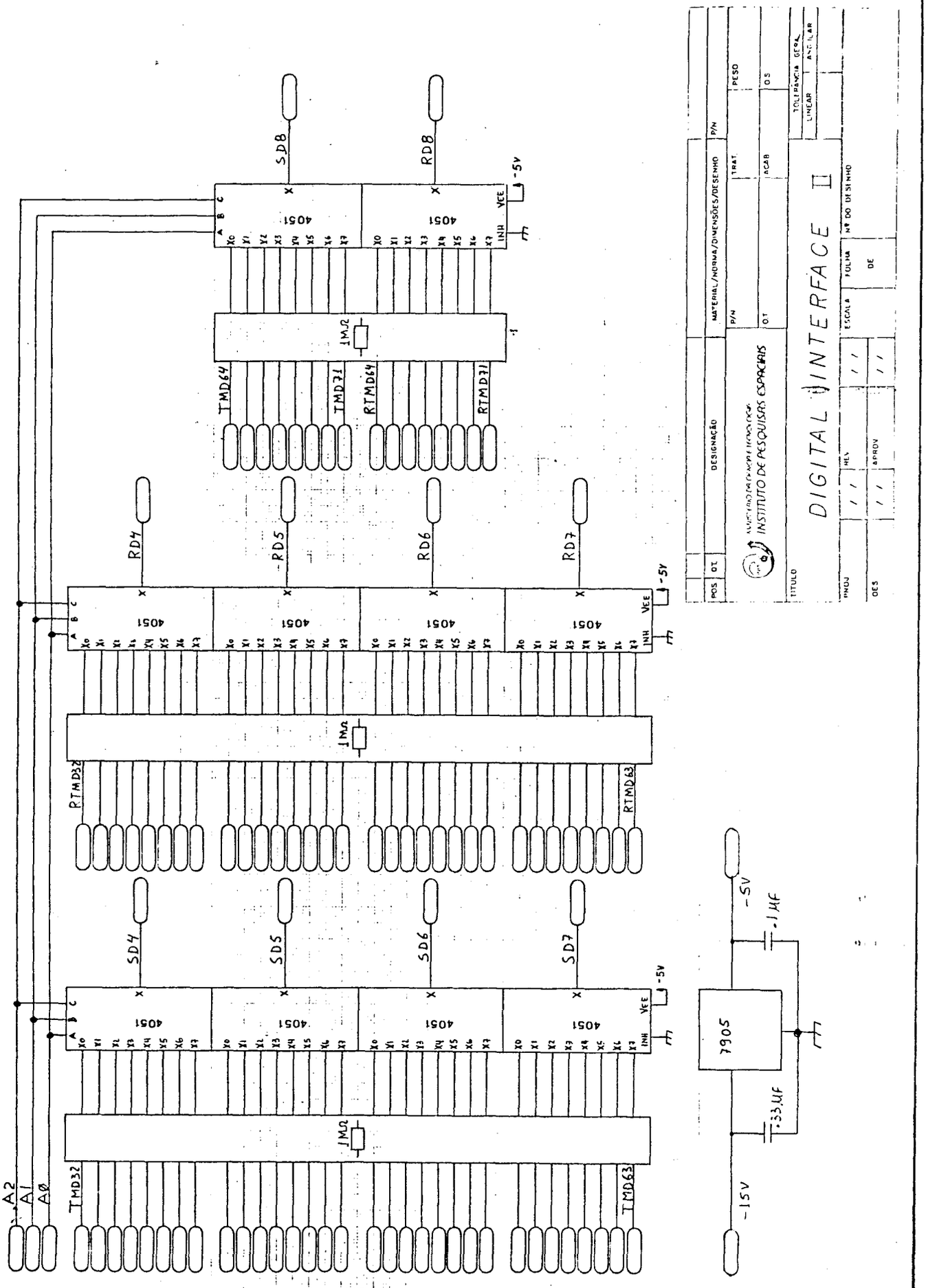

+5VUAC
-5VUAC
TUAC
RAUAC
SAUAC
74051
IM
LINHA 31
LINHA 63
EUAC 88
EUAC 48
EUAC 58
EUAC 68
EUAC 78
THA 32
THA 62
ST
DESIGNAÇÃO
MATERIAL/NORMA/DIMENSÕES/DESENHO
P/N
PESO
ESCALA
FOLHA
Nº DO DESENHO
INSTITUTO DE PESQUISAS ESPACIAIS

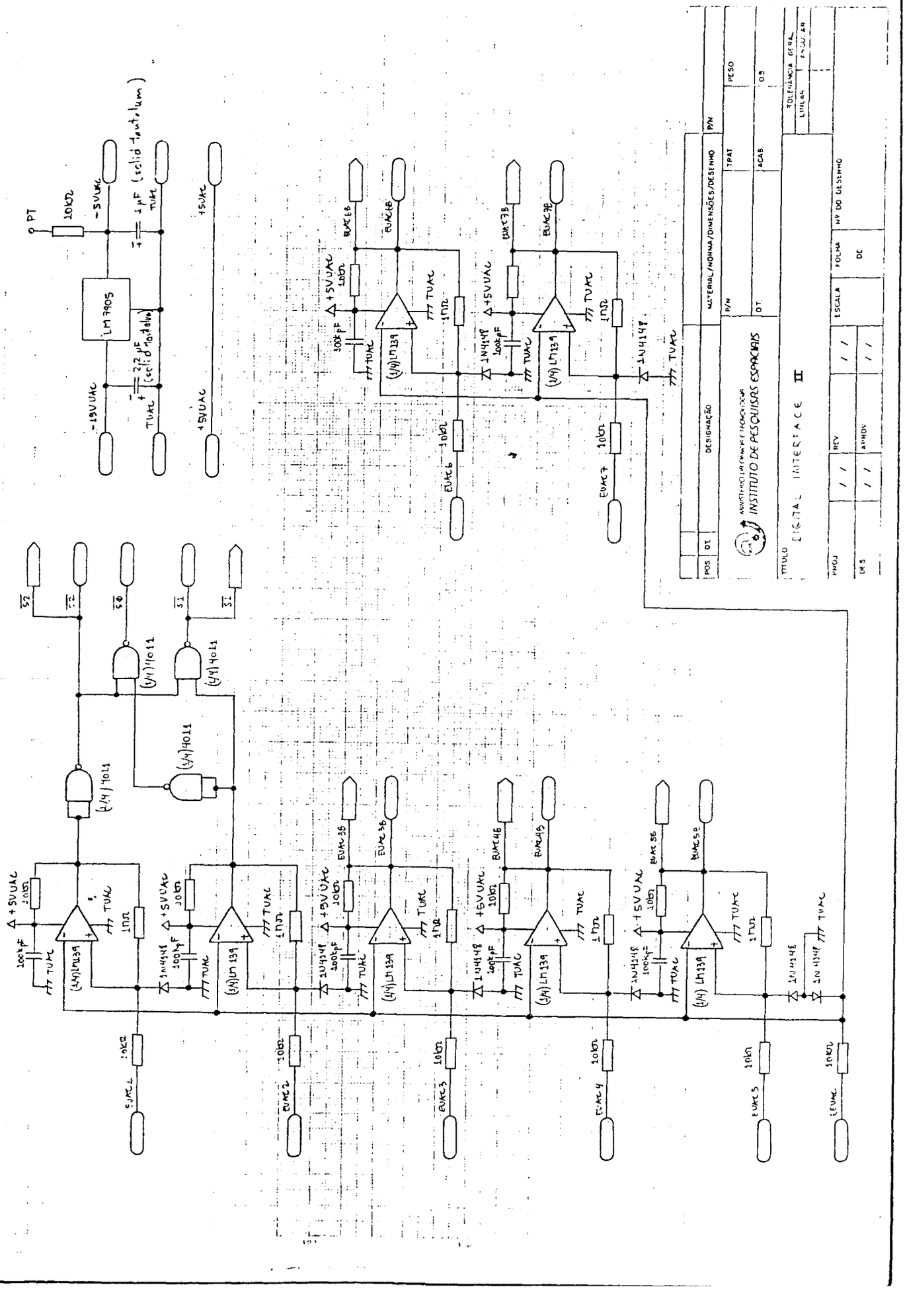

RA8
RA9
RA10
RA11
4051
-5V
RMA
RTMA64
RTMA95
SA8
SA9
SA10
SA11
TMA64
TMA95
A5
A4
A3
ANALOG INTERFACE III
INSTITUTO DE PESQUISAS ESPACIAIS

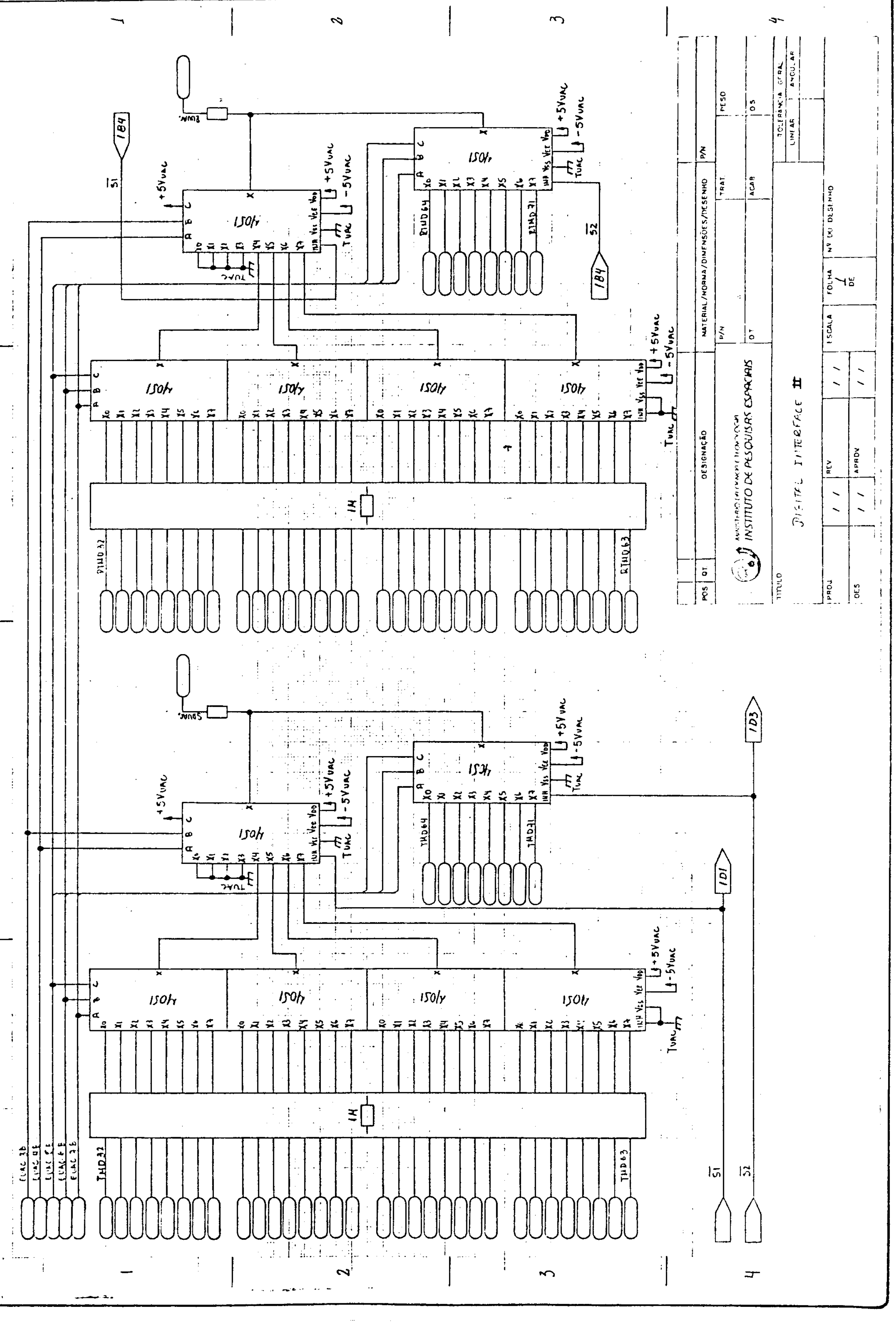

BAUAC
SAUAC
TUAC
+5VUAC
-5VUAC
150h
1H
EIHA 64
EIHA 95
SIHA 64
SIHA 95
CUAC 3B
CUAC 4B
CUAC 2B
CUAC 6B
CUAC 1B
DESIGNAÇÃO
MATERIAL/NORMAS/DIMENSÕES/DESENHO
TRAT
ACAB
PESO
ESCALA
FOLHA
Nº DO DESENHO
REV
APROV
TÍTULO
ANALOG INTERFACE III
INSTITUTO DE PESQUISAS ESPACIAIS

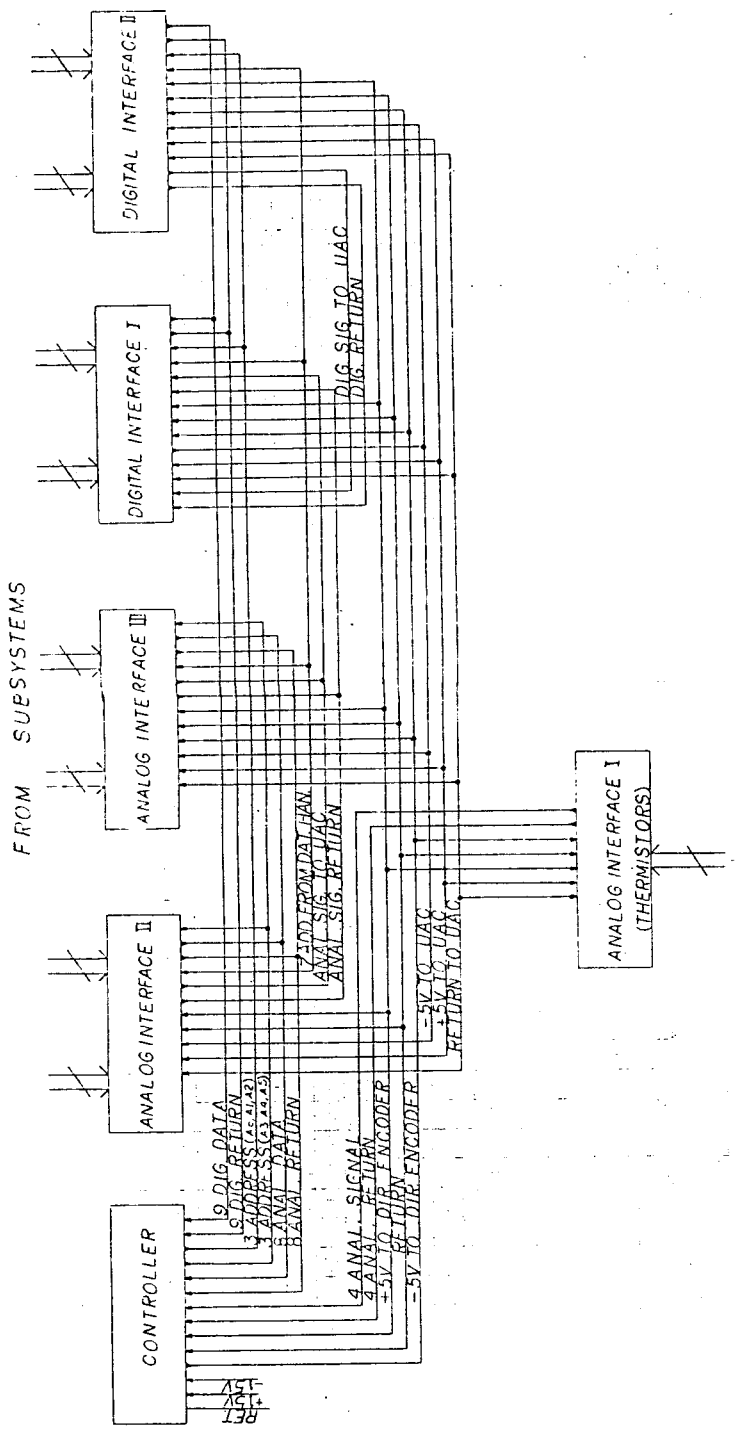

DIGITAL INTERFACE I
INSTITUTO DE PESQUISAS ESPACIAIS
4051
4050
3K
2K
-5V
PSK

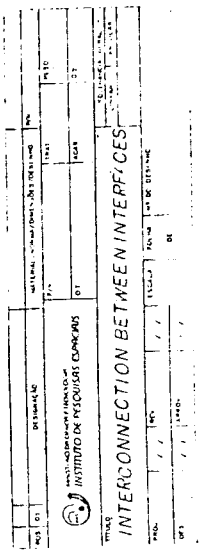

RDUAC
SDUAC
TUAC
+5VUAC
-5VUAC
4051
1M
2M
RINDØ
RIND31
TMDØ
TMD31
DIGITAL INTERFACE I
INSTITUTO DE PESQUISAS ESPACIAIS

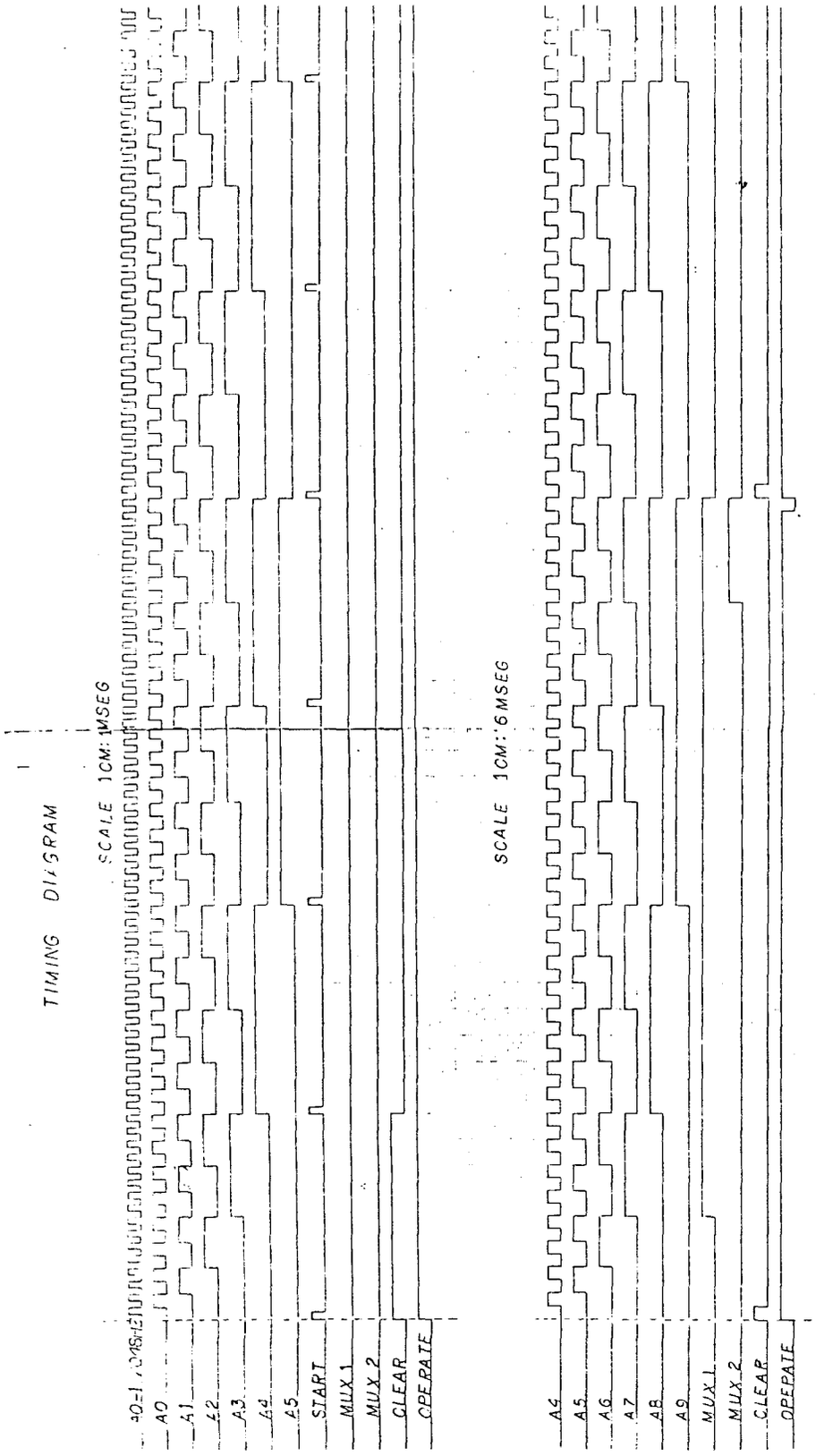

SD8
RD8
-5V
4051
TMD64
TMD71
RTMD64
RTMD71
RD4
-RD5
RD6
RD7
RTMD32
RTMD63
SD4
SD5
SD6
SD7
TMD32
TMD63
A2
A1
A0
DIGITAL I/INTERFACE II
INSTITUTO DE PESQUISAS ESPACIAIS
DESIGNAÇÃO
MATERIAL/NORMA/DIMENSÕES/DESENHO
P/N
ESCALA
FOLHA
Nº DO DESENHO
7905
-1,5V
.1 µF
33 µF

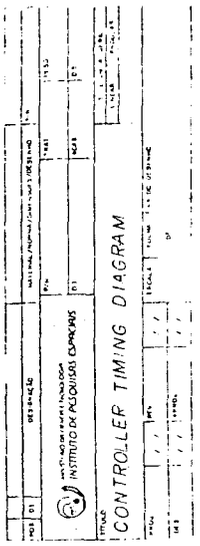

PT
10KΩ
-5VUAC
4μF (solid tantalum)
TUAC
LM 7905
2,2 μF (solid tantalum)
-15VUAC
+5VUAC
+15VUAC
EUAC1
EUAC2
EUAC3
EUAC4
EUAC5
EUAC6
EUAC7
EUAC8
EUAC9
EUAC10
EUAC11
EUAC12
EUAC13
EUAC14
EUAC15
EUAC16
(1/4) LM139
1N4148
100pF
1KΩ
10KΩ
(1/4) 4011
S2
S3
S4
S1
S5
DESIGNAÇÃO
MATERIAL/NORMA/DIMENSÕES/DESENHO
INSTITUTO DE PESQUISAS ESPACIAIS
INTERFACE DIGITAL II


4051
4051
4051
4051
4051
4051
4051
4051
4051
4051
4051
4051
1H
1H
+5VAC
-5VAC
TVAC
1B4
1B4
1D1
1D3
S1
S2
RTHD64
RTHD21
RTHD32
RTHD63
THD64
THD21
THD32
THD63
INSTITUTO DE PESQUISAS ESPACIAIS
DIGITAL INTERFACE II


FROM SUBSYSTEMS
DIGITAL INTERFACE II
DIGITAL INTERFACE I
ANALOG INTERFACE III
ANALOG INTERFACE II
CONTROLLER
ANALOG INTERFACE I
(THERMISTORS)
DIG SIG TO UAC
DIG RETURN
ANAL SIG TO UAC
ANAL SIG RETURN
-5V TO UAC
+5V TO UAC
RETURN TO UAC
9 DIG DATA
5 DIG RETURN
3 ADDRESS (A5,A4,A3)
3 ADDRESS (A2,A1,A0)
8 ANAL DATA
8 ANAL RETURN
4 ANAL SIGNAL
4 ANAL RETURN
+5V TO DIR ENCODER
RETURN
-5V TO DIR ENCODER
+15V
-15V
RET


INTERCONNECTION BETWEEN INTERFACES
INSTITUTO DE PESQUISAS ESPACIAIS


TIMING DIAGRAM
SCALE 1CM:1MSEG
A0
A1
A2
A3
A4
A5
START
MUX 1
MUX 2
CLEAR
OPERATE
SCALE 1CM:6MSEG
A4
A5
A6
A7
A8
A9
MUX 1
MUX 2
CLEAR
OPERATE


CONTROLLER TIMING DIAGRAM

CONSELHO NACIONAL DE DESENVOLVIMENTO CIENTÍFICO E TECNOLÓGICO
INSTITUTO DE PESQUISAS ESPACIAIS

PROPOSTA PARA PUBLICAÇÃO

DATA: 31.07.86

IDENTIFICAÇÃO

TÍTULO: THE DIRECT TELEMETRY ENCODER : A DETAILED DESCRIPTION

AUTORIA:
Alderico R. de Paula Junior
Ricardo de Azevedo Mendes
Fernando Antonio Pessotta

PROJETO/PROGRAMA: SUBORD

DIVISÃO: DIA

DEPARTAMENTO: DCA

DIVULGAÇÃO ☐ EXTERNA ☒ INTERNA MEIO: Restrita

REVISÃO TÉCNICA

REVISOR TÉCNICO: Eduardo W. Bergamini

RECEBI EM: _____ REVISADO EM: _____

OBSERVAÇÕES: ☐ NÃO HÁ ☐ VER VERSO

DEVOLVI EM: _____ EDUARDO WHITAKER BERGAMINI Chefe do Dept.º de Computação em Aplicações Especiais DCA ASSINATURA

APROVAÇÕES

APROVADO: ☒ SIM ☐ NÃO ☐ VER VERSO

4/11/86 DATA — Alderico CHEFE DIVISÃO

APROVADO: ☐ SIM ☐ NÃO ☐ VER VERSO

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REVISÃO DE LINGUAGEM

Nº : 332 PRIORIDADE: 1

DATA: 1-8-86

REVISADO ☐ COM ☐ SEM CORREÇÕES ☐ VER VERSO

POR: Paulia Prado de Carvalho

4.8.86 DATA — Paulia P. Carvalho ASSINATURA

DATILOGRAFIA

O(S) AUTOR(ES) DEVE(M) MENCIONAR NO VERSO, OU ANEXAR NORMAS E/OU INSTRUÇÕES ESPECIAIS

RECEBIDO EM: Julho/86

CONCLUÍDO EM: Julho/86

DATILÓGRAFA : Marta

ASSINATURA

PARECER

FAVORÁVEL : ☐ SIM ☐ NÃO ☐ VER VERSO

_____ DATA _____ RESPONSÁVEL/PROGRAMA

EM CONDIÇÕES DE PUBLICAÇÃO EM: _____ _____ AUTOR RESPONSÁVEL

AUTORIZO A PUBLICAÇÃO : ☐ SIM ☐ NÃO

DIVULGAÇÃO ☐ INTERNA ☐ EXTERNA MEIO: _____

OBSERVAÇÕES : _____

_____ DATA _____ DIRETOR

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